85

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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ZAGORIN O'BRIEN & GRAHAM, L.L.P.
7600B N. CAPITAL OF TEXAS HWY.
SUITE 350
AUSTIN, TX 78731

EXAMINER	
PAPPAS, PETER	
ART UNIT	PAPER NUMBER
2671	

DATE MAILED: 11/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/090,507	SELL, JOHN V.
	Examiner	Art Unit
	Peter-Anthony Pappas	2671

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18,20-31 and 33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *18,20-23,26,27,30 and 31* is/are allowed.

6)☒ Claim(s) *1-17,24,25,28 and 29* is/are rejected.

7)☒ Claim(s) *33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 March 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

1. The previously indicated allowability of claims 28-29 is withdrawn in view of the new grounds of rejection cited in the present Office action.

2. Claim 33 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

3. Claims 18-23, 26-27 and 30-31 are allowed.

4. In regards to claim 30 the prior art of record does not disclose or suggest each of the entries of the hierarchical image depth buffer including at least one pair of near and far values and at least one un-paired near value.

5. In regards to claim 31 the prior art of record does not disclose or suggest each of the entries of the hierarchical image depth buffer including at least one pair of near and far values and at least one non-paired near value.

Specification

6. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: The specification teaches a "...a three level hierarchy for initialization purposes. The first two levels are the depth information hierarchy. The third level consists of an initialization flag for each 16 x 8 'Superblock' of 128 pixels. Superblockinit flags are 'cached' in a small number of 64 byte buffers in the graphics engine" (pages 24-25, ¶ 1079). However, the specification fails to support "...a third

level hierarchical buffer containing a plurality of initialization flags..." (page 7, lines 9-12).

Drawings

7. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "...a third level hierarchical buffer containing a plurality of initialization flags..." (page 7, lines 9-12) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-2, 5-8, 10-15, 24 and 28-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Greene et al. (U.S. Patent No. 5, 579, 455).

10. In regards to claim 1 Greene et al. teaches a computer system (computer graphics processing system), comprising CPU 120, memory 104 and graphics coprocessor 110, wherein said graphics coprocessor 110 is able to offload, from CPU 102, many of the memory-intensive tasks required for manipulating graphics data in memory 104 (column 8, lines 22-47; Fig. 1). A display buffer (image depth buffer), which can be stored in memory 104, comprises memory elements 302, wherein each display cell element contains a display cell value which represents an attribute of the appearance of the respective display cell (column 9, lines 12-19). Each of the said display cells has attributes associated with it such as color and a depth value (column 9, lines 1-5).

Greene et al. teaches that the basic idea of the Z-pyramid is to use a conventional depth buffer (Z-buffer) as the finest level in the pyramid and then combine four Z values at each level into one Z value at the next coarser level (column 5, lines 51-59). A depth buffer 502 (hierarchical image depth buffer) is divided into four levels of granularity or resolution designated 504, 506, 508 and 510. In the finest granularity

level 504 said depth buffer has a depth value corresponding to each of the display cells (pixels) 204 (column 5, lines 51-59; column 10, lines 8-27; Fig. 5, Fig. 5A). Each depth element 512 (data item) can contain both Z-max (farthest depth value) elements and Z-min (nearest depth value) elements (column 11, lines 4-12).

Granularity levels 504, 506, 508 and 510 of said depth buffer 502 are comprised of sixty-four, sixteen, four and one depth element(s) 512, respectively. Each depth element in level 506 represents four depth elements from level 504. Each depth element in level 508 represents sixteen depth elements from level 504 and four depth elements from level 506. Each depth element in level 510 represents sixty-four depth elements from level 504, sixteen depth elements from level 506 and four depth elements from 508 (column 10, lines 8-7, column 9, lines 1-3; Fig. 5-6). Thus, for example, at granularity level 508 a single given depth element 512 is considered to represent the Z-min and Z-min for four depth elements 512 (multiple near and far) from granularity level 506 or instead represent the Z-min and Z-min for sixteen depth elements 512 (multiple near and far) from granularity level 504.

11. In regards to claim 2 Greene et al. teaches that in step 608 the depth buffer 502 is initialized by writing the farther depth value permitted into all Z-max elements 512. It is inherent that when initializing a depth (Z) buffer, which stores both Z-min and Z-max values, that said Z-min and Z-max values for a display cell of a given display area (comprised of a plethora of display cells) would both be initialized to background pixel depth values. Thus, once a primitive is displayed on said display area and covers a portion of the background pixels, said remaining background pixels used to initialize

said Z-min and Z-max values would represent a subset of the plurality of corresponding pixels of said display area.

12. In regards to claim 5 Greene et al. teaches of an 8x8 display buffer (column 9, lines 12; Fig. 3), comprising sixty-four display cells 204. Levels 506, 508 and 510 of said depth buffer 502 are comprised of sixteen depth elements 512, four depth elements 512 and one depth element 512, respectively. Each depth element 512 in level 506 represents four depth elements 512 from level 504, each depth element 512 in level 508 represents sixteen depth elements 512 from level 504 and the depth element 512 in level 510 represents all sixty-four depth elements 512 from level 504, which also is the size of said display buffer (column 10, lines 8-7, column 9, lines 1-3; Fig. 5-6). Thus, it is noted that depth buffer 502 at levels 506, 508 and 510 is considered substantially less then the size of said display buffer.

13. In regards to claim 6 Greene et al. teaches an 8x8 display buffer (column 9, lines 12; Fig. 3), thus comprising sixty-four display cells 204. Levels 508 and 510 of said depth buffer 502 are comprised of four depth elements 512 and one depth element 512, respectively. Each depth element 512 in level 508 represents sixteen depth elements 512 from level 504 and the depth element 512 in level 510 represents all sixty-four depth elements 512 from level 504, which also is the size of said display buffer (column 10, lines 8-7, column 9, lines 1-3; Fig. 5-6). Thus, it is noted that said depth buffer 502 at levels 508 and 510 is considered less then one-fourth the size of said display buffer.

14. In regards to claim 7 Greene et al. teaches an 8x8 display buffer (column 9, lines 12; Fig. 3), thus comprising sixty-four display cells 204. Level 508 of said depth buffer

502 is comprised of four depth elements 512. Each depth element 512 in level 508 represents (corresponds to) sixteen depth elements 512 from level 504, which also is the size of said display buffer (column 10, lines 8-7, column 9, lines 1-3; Fig. 5-6).

15. In regards to claim 8 Greene et al. teaches that in order to use the Z-pyramid to test (detect) the visibility of a polygon, the finest-level sample of the pyramid whose corresponding image region covers the screen-space bounding box of the polygon is found. If the nearest Z value of the polygon is farther away than the sample in the Z-pyramid, the polygon is entirely hidden (column 5, lines 65-67, column 6, lines 1-8).

16. In regards to claim 10 the rationale disclosed in the rejection of claim 1 is incorporated herein. Green et al. teaches a "prove primitive hidden" routine 1706 (Fig. 18; Fig. 20). In step 1802 the finest granularity depth element in depth buffer 502, which fully covers the primitive, is determined. In step 1802 the level of the said depth element is noted and in step 1804 the depth of the nearest point (pixel) in the primitive (object to be rendered) is determined. Said determinations and a reference to said primitive are passed to a recursive procedure 1808. Recursive procedure 1808 establishes a visibility determination for said primitive, in respect to said nearest point, via comparison between data stored in said depth buffer 502 and the parameters passed to said recursive procedure 1808 (column 16, lines 61-67, column 17, lines 1-67, and column 18, lines 1-8).

17. In regards to claim 11 Greene et al. teaches if a primitive fails to be found hidden in step 2002 said primitive is scan converted to determine the display cells (surface cells) it covers. Each surface cell is rendered if it is visible relative to objects which

have previously been written. This visibility check is performed by comparing the depth of the current surface cell to the depth values currently in the depth buffer 502 at the finest level for the corresponding display cell (column 18, lines 56-67, column 19, lines 1-12).

18. In regards to claim 12 Greene et al. teaches that if said display cell is not hidden then the color or other attributes of said current surface cell are written into the display buffer (frame buffer) of the corresponding display cell (column 19, lines 13-20).

19. In regards to claim 13 Greene et al. teaches if said primitive is proven to be definitely hidden, as per routine 1706, then routine 1610 returns (step 2004) without rendering anything (column 18, lines 56-61). Thus, it is noted that said nearest point of said primitive is considered discarded.

20. In regards to claim 14 the rationale disclosed in the rejection of claim 13 is incorporated herein. Greene et al. teaches that if step 2002 fails to prove the primitive hidden, a step 2006 scan converts the primitive in a conventional manner to determine the surface cells that it contains. Step 2010 determines whether the particular surface cell is hidden. This is a conventional determination made by comparing the depth of the current surface cell to the depth value current in the depth buffer 502 at the finest level of the corresponding display cell (column 18, lines 62-67, and column 19, lines 1-12; Fig. 20).

21. In regards to claim 15 Greene et al. teaches updating the depth buffer 502 (steps 2020 and 2022) in regards to a Z-max and Z-min element (column 19, lines 21-37; Fig. 20).

22. In regards to claim 24 the rationale disclosed in the rejection of claim 1 is incorporated herein.

23. In regards to claim 28 the rationale disclosed in the rejection of claim 1 is incorporated herein.

24. In regards to claim 29 the rationale disclosed in the rejection of claim 1 is incorporated herein.

Claim Rejections - 35 USC § 103

25. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

26. Claims 3, 4, 16-17 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Greene et al. (U.S. Patent No. 5, 579, 455), as applied to claims 1-2, 5-8, 10-15, 24 and 28-29, in view of in view of Dawson (U.S. Patent No. 6, 567, 099 B1).

27. In regards to claim 3 Greene et al. fails to explicitly teach the hierarchical image depth buffer further comprises at least one flag. Dawson teaches that a standard Z-buffer has a certain amount of memory set aside to store data for each pixel, wherein said data includes a color triplet, a Z-distance value and some bit flags (column 6, lines 34-43). Dawson teaches updating said bit flags () and that bit flags are used to determine (via their status) various pixel properties (column 7, lines 21-35).

It would have been obvious to one skilled in the art, at the time of the applicant's invention, to incorporate various elements of a standard Z-buffer, such as bit flags, into a buffer which is based upon a Z-buffer, such as a depth buffer 502 taught by Greene et al., because said depth buffer is built upon the properties of a Z-buffer and thus by incorporating said bit flags into said depth buffer it would provide additional information as to the presence or absence of data for given data entries in said depth buffer, allowing for the storage of additional information.

28. In regards to claim 4 Greene et al. teaches that a surface primitive 206 covers (occludes) a portion of seven of the display cells 204 (column 8, lines 56-66; Fig. 2). Greene et al. fails to explicitly wherein the first subset corresponds to a set of foreground pixels.

It is well known that if a given object, which is to be displayed, completely covers a display area or a portion of a given display area that said area is occluded by said object (official notice; see MPEP § 2144) and thus, it would have been obvious to one skill in the art, at the time of the applicant's invention, that if a surface primitive completely covers a pixel or group of pixels in a given display area, the respective Z-min and Z-max values for said covered pixel(s) would be determined by the surface primitive (foreground pixels), because for a given completely covered pixel there would be no visible background and thus only one depth value to assign.

29. In regards to claim 16 Greene et al. fails to explicitly teach the data items include a flag and a step of checking a status of the flag. The rationale disclosed in the rejection of claim 3, in regards to the data items including a flag, is incorporated herein.

30. In regards to claim 17 Greene et al. fails to explicitly teach the data items include a flag and a step of updating a status of a flag. The rationale disclosed in the rejection of claim 3, in regards to the data items including a flag, is incorporated herein

31. In regards to claim 25 the rationale disclosed in the rejection of claim 4 is incorporated herein. It is noted that said surface primitive 206 covering a portion of display cells is considered a first foreground object.

32. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Greene et al. (U.S. Patent No. 5, 579, 455), as applied to claims 1-2, 5-8, 10-15, 24 and 28-29, in view of in view of Greene (U.S. Patent No. 6, 636, 215 B1).

33. In regards to claim 9 Greene et al. (U.S. Patent No. 5, 579, 455) teaches a central processor (CPU) 102, graphics coprocessor 110 and a memory 104 (Fig 1.). Green et al. fails to explicitly teach a memory controller, where a graphics processor is coupled to said memory controller and responsive to the central processor (CPU). Green (U.S. Patent No. 6, 636, 215 B1) teaches a host processor (CPU) 110, memory controller 3314, which manages access to the host memory 114 by a number of potential masters including the host processor 110 and the AGP bus 3310, host memory 3312 and graphics system 100, which includes a graphics processor 3316. Said graphics processor 3316 is connected to said memory controller 3314 via a AGP bus 3310 (Fig. 33).

It would have been obvious to one skilled in the art, at the time of the applicant's invention, to incorporate a memory controller for the management of accessing host memory, as taught by Greene, into the system as taught by Greene et al., because it

would have been conventional to implement a memory controller, in a system which utilizes memory, to serve as an arbiter for the transfer of data in memory between the various components of a given system.

Response to Amendment

34. In regards to the 35 U.S.C. 112 rejection for claim 17 said rejection has been withdrawn in lieu of applicant's remarks.

35. In response to applicant's remarks that Greene et al. fails to teach the limitations of amended claims 1 and 10 it is noted that said claim fails to limit the data items for a given hierarchical image depth buffer to a nearest depth value and farthest depth value for a first subset and nearest depth value for a second subset. Greene et al. teaches storing a plurality of Z-min and Z-man values, per granularity level (subset), for depth elements 512, as disclosed in the present rejection for claims 1 and 10, respectively.

36. In response to applicant's remarks that Greene et al. fails to teach the limitations of amended claim 24 Greene et al. teaches that granularity levels 504, 506, 508 and 510 of said depth buffer 502 are comprised of sixty-four, sixteen, four and one depth element(s) 512, respectively. Each depth element in level 506 represents four depth elements from level 504. Each depth element in level 508 represents sixteen depth elements from level 504 and four depth elements from level 506. Each depth element in level 510 represents sixty-four depth elements from level 504, sixteen depth elements from level 506 and four depth elements from 508 (column 10, lines 8-7, column 9, lines 1-3; Fig. 5-6). Thus, for example, at granularity level 508 a single given depth element 512 is considered to represent the Z-min and Z-min for four depth elements 512

(multiple near and far) from granularity level 506 or instead represent the Z-min and Z-min for sixteen depth elements 512 (multiple near and far) from granularity level 504.

37. It is noted that if claim 1 was amended to include the limitations of dependent claims 2 and 4, resulting in the canceling of claims 2 and 4, said amended claim would overcome the prior art of record.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Peter-Anthony Pappas whose telephone number is 703-305-8984. The examiner can normally be reached on M-F 10:00am-6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Zimmerman can be reached on 703-305-9798. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Peter-Anthony Pappas
Examiner
Art Unit 2671

PAP

Mark Zimmerman

MARK ZIMMERMAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600